REMARKS

These Remarks are in reply to the Office Action mailed October 30, 2008. Claims 1-19 were pending in the Application prior to the outstanding Office Action. Claims 1-8 and 13-19 are being amended, no claims are being cancelled and no new claims are being added, leaving claims 1-19 for the Examiner's consideration. In view of the above amendments and the remarks below, Applicants respectfully request that the rejections be reconsidered and withdrawn, and that a Notice of Allowance be issued.

I. Summary of Claim Rejections Under 35 U.S.C. 103

Claims 1-4, 8, and 10-16 were rejected under 35 U.S.C. 103(a) for allegedly being unpatentable over U.S. Patent Publication No. 2002/0122518 to Yasuda et al. (hereinafter referred to as "Yasuda") in further view of U.S. Patent No.7,099,426 to Cory et al. (hereinafter referred to as "Cory") and further in view of U.S. Patent No. 5,390,180 to Reilly (hereinafter referred to as "Reilly").

Claim 9 was rejected under 35 U.S.C. 103(a) for allegedly being unpatentable over the combination of Yasuda, Cory and Reilly as applied to claim 8 above, and further in view of U.S. Patent No. 7,302,396 to Cooke (hereinafter referred to as "Cook").

II. Allowable Subject Matter

Applicants thank the Examiner for indicating that claims 5-7 and 17-19 would be allowable if rewritten in independent form.

Claims 5 and 17 have been redrafted in independent form.

Claims 6 and 7 depend from independent claim 5. Claims 18 and 19 depend from independent claim 17.

All of these claims should be in condition for allowance.

(a discussion of the claims begins on the next page)

III. Discussion of Claims

1. Claim 1

Claim 1 requires, inter alia, that

each of a plurality of channels includes

> "a buffer management unit ... configured to control a rate at which samples are read from the input buffer to achieve a target difference between the values of the read and write pointers;

wherein for a first one of the channels, the target difference comprises a predetermined value;

wherein for the remainder of the channels, the target difference comprises the actual difference between the values of the read and write pointers of the first one of the channels; and

wherein for each channel the buffer management unit is configured to read samples from the input buffer in an order in which the samples were written to the input buffer without skipping or re-reading any of the samples stored in the input buffer."

Applicants respectfully assert that the cited references, alone or in combination, do not teach or suggest the above features, as explained below.

Cory discusses both a master elastic buffer and slave elastic buffers. For this discussion, Applicants assume that the Examiner is asserting that Cory's master elastic buffer is part of a master channel that is analogous to the claimed "first one of the channels"; and that Cory's slave elastic buffers are part of slave channels that are analogous to the claimed "the remainder of the channels".

1.a Cory does not teach or suggest that each of a plurality of channels includes "a buffer management unit ... configured to control a rate at which samples are read from the input buffer to achieve a target difference between the values of the read and write pointers; wherein for a first one of the channels, the target difference comprises a predetermined value" as required by claim 1

It was asserted in the Office Action, that column 19, lines 7-23 of Cory teaches that Cory's controls a read pointer to achieve a target difference for a first one of the channels.

Applicants respectfully disagree. For the convenience of the Examiner, column 18, line 61 – column 19 line 31 (which includes Column 19, lines 7-23) of Cory is quoted verbatim below (with emphasis added).

> "Operational control circuit 211 also ensures that clock correction operations are handled properly by read control circuit 213. As input data stream Din is written to memory space 220, operational control circuit 211 monitors input data stream Din and write address Waddr to keep track of the locations of correction sequences (and also channel alignment blocks) within memory space 220. **Operational control circuit 211 evaluates the "fullness" of memory space 220 (as indicated by the difference between the read and write addresses), and it determines whether to do an accelerating or delaying clock correction, or continue reading normally when read address Raddr_a or read address Raddr_b reaches a correction sequence**.
>
> To execute these various actions, operational control circuit 211 provides a plurality of control signals to read control circuit 213. To initiate clock correction operations, operational control circuit 211 can generate clock correction signals CC_enb and CC_enb2, and to specify the appropriate clock correction increments, operational control circuit 211 can generate address/increment signals incr_addr and incr_addr2. Note that address/increment signals incr_addr and incr_addr2 can specify either an increment (positive or negative) by which the current address is modified, or an absolute address that replaces the current address. Operational control circuit 211 can also provide an optional stagger control signal STAG to control clock correction operations taking place across multiple read clock cycles. Finally, operational control circuit 211 can provide a channel bonding signal CB_load to control channel bonding operations, to be discussed in a subsequent section. Note that clock correction signal CC_enb2, address/increment signal incr_addr2 and stagger control signal STAG are shown as optional (using dotted lines) and can therefore represent any number of additional control signals required to perform the clock correction operations described previously. Note further that circuit 211 can maintain internal copies of write address Waddr and read address Raddr_b to ensure generation of the elastic buffer control signals in a timely fashion."

In the first paragraph quoted above (i.e., Column 18, line 61 – Column 19, line 6), Cory explains that its operational control circuit can evaluate the fullness of its memory space based on the difference between the read and write addresses. However, this portion of Cory never states that it controls a rate at which samples are read from an input buffer to achieve a target difference between the values of the read and write pointers/addresses for a one of the channels (e.g., Cory's master channel), where **the target difference comprises a predetermined value**, as is required by claim 1. In other words, while Cory determines a difference between read and write addresses, Cory does so to determine the fullness of the memory, **NOT** to control a rate at which samples are read from the buffer of Cory's master channel to achieve a target difference in the master channel that is a predetermined value.

Further, in the first paragraph quoted above, Cory states that it determines whether to perform an accelerating or delaying clock correction, or continue reading normally "when read address Raddr_a or read address Raddr_b reaches a **correction sequence**". As defined in Cory at Column 2, lines 21-23, a "correction sequence" is defined as the smallest set of data blocks that may be omitted or added for clock correction operations.

In the second paragraph quoted above (i.e., Column 19, lines 7 – 31), Cory explains that address/increment signals (incr_addr and incr_addr2) can specify either an increment (positive or negative) by which a current address is modified, or an absolute address that replaces the current address. However, this portion of Cory never states that the current address is modified or replaced in order to achieve a target difference between the values of the read and write pointers/addresses for a one of the channels (e.g., Cory's master channel), where **the target difference comprises a predetermined value**, as is required by claim 1.

Further, none of the other applied references appear to teach or suggest this deficiency of Cory.

1.b Cory does not teach or suggest "wherein for the remainder of the channels, the target difference comprises the actual difference between the values of the read and write pointers of the first one of the channels" as required by claim 1

Claim 1 further specifies "wherein for the remainder of the channels, the target difference comprises the actual difference between the values of the read and write pointers of the first one of the channels". Thus if the predetermine value of the target difference is, e.g., 100, but the actual difference between the read and write pointers of the first one of the channels is 105, then for the other channels (i.e., the remainder of the channels) the buffer management unit is configured to control the rate at which samples are read from the input buffer (of those remaining channels) to achieve a difference of 105, to attempt to synchronize the remainder of the channels with the first one of the channels. This is useful because it is better to have the phase of a plurality of channels similarly offset from a desired phase than to have all the channels close to the desired phase but offset from each other. In other words, in the embodiment of claim 1, the remainder of the channels (e.g., the slave channels) will track the offset of the first one of the channels (e.g., the master channel) in order to match the phase delay through all of the channels of the system, which is useful because for an audio system time alignment is important. Thus,

this approach maintains alignment even if a time base of the first one of the channels (e.g., the master channel) is drifting.

It was asserted in the Office Action that Cory teaches "wherein for the remainder of the channels, the target difference comprises the actual difference between the values of the read and write pointers of the first one of the channels" at Column 29, lines 56-66. Applicants respectfully disagree. For the convenience of the Examiner, Column 29, lines 56-66 of Cory is quoted verbatim below.

> "Note that after completion of a channel bonding operation, the resulting data alignment could be destroyed if all the elastic buffers executed different clock corrections (type and/or timing). Therefore, according to an embodiment of the invention, master elastic buffer 200(1) can maintain data alignment produced by controlling clock correction operations for all slave elastic buffers as well as for itself. Controller 210(1) in master elastic buffer 200(1) could control channel alignment and clock correction by means of the CC_enb, CB_load, STAG, and incr_addr signal connections as shown in FIG. 2d. According to an embodiment of the invention, these signals could be asserted early and buffered inside controllers 210(1) and 210(2) for subsequent assertion at an appropriate time, thereby accommodating signal routing delays between elastic buffers."

The above quoted portion of Cory explains that the master elastic buffer can maintain data alignment for all the slave elastic buffers and itself by means of the CC_enb, CB_load, STAG, and incr_addr signal. CC_enb is a clock correction signal, CB_load is a channel bonding signal, STAG is stagger control signal, and incr_addr is an address increment signal. Thus, the above quoted section of Cory merely explains that the master elastic buffer can control itself and the slave buffers by controlling clocks, by channel bonding, by staggering and/or by incrementing addresses. However, this portion of Cory, nor any other portion of Cory, teaches that the rate at which samples are read from the input buffers of the remainder of the channels (presumably the slave channels) is controlled specifically to achieve the actual difference between the values of the read and write pointers of the first one of the channels (presumably the master channel).

Further, none of the other applied references appear to teach or suggest this deficiency of Cory.

1.c Reilly does not teach or suggest a "for each channel the buffer management unit is configured to read samples from the input buffer in an order in which the samples were written to the input buffer without skipping or re-reading any of the samples stored in the input buffer" as required by claim 1

It was admitted in the Office Action that Yasuda and Cory do not teach these features of claim 1. However, it was alleged the Reilly teaches such features, and that one of ordinary skill in the art would have known how to modify the combination of Yasuda and Cory to teach that "for each channel the buffer management unit is configured to read samples from the input buffer in an order in which the samples were written to the input buffer without skipping or re-reading any of the samples stored in the input buffer", where each channel of a plurality of channels includes such a buffer management unit. Applicants respectfully disagree, as explained below.

Reilly only discusses how to buffer data in a single channel, which is quite different that buffering data in multiple channels while attempting to align the phases of the multiple channels. In other words, assuming for arguments sake that Reilly indeed teaches how to "read samples from the input buffer in an order in which the samples were written to the input buffer without skipping or re-reading any of the samples stored in the input buffer", Reilly could still not be used to modify the suggested combination of Yasuda and Cory to, for each of a plurality of channels "control a rate at which samples are read from the input buffer to achieve a target difference between the values of the read and write pointers; wherein for a first one of the channels, the target difference comprises a predetermined value; wherein for the remainder of the channels, the target difference comprises the actual difference between the values of the read and write pointers of the first one of the channels; and wherein the buffer management unit (in each of the plurality of channels) is configured to read samples from the input buffer in an order in which the samples were written to the input buffer without skipping or re-reading any of the samples stored in the input buffer" as required by claim 1.

For at least the reasons specified above, Applicants respectfully request that the rejection under 35 U.S.C. 103(a) of claim 1 be reconsidered and withdrawn. If the Examiner is to maintain this rejection, Applicants respectfully request that the Examiner explain in more detail how the Examiner is interpreting the cited references to teach the above discussed features of claim 1.

2. Claims 2-4

Claims 2-4 depend from claim 1. Applicants assert that these claims are patentable for at least the reason that they depend from claim 1, as well as for the features that they add.

3. Claims 5-7

Allowable claim 5 has been redrafted in independent form, such that it includes the features of claims 1, 3 and 4. Claims 6 and 7 depend from claim 5. Applicants respectfully request that these claims be allowed.

4. Claim 8

In the rejection of claim 8, the Office Action said to see the preceding argument with respect to claim 1. Applicants respectfully assert that claim 8 is patentable over the cited references, alone or in combination, for similar reasons to those discussed above with regards to claim 1. Accordingly, Applicants respectfully request that the rejection of claim 8 be reconsidered and withdrawn.

5. Claims 9-13

Claims 9-13 depend from claim 8. Applicants assert that these claims are patentable for at least the reason that they depend from claim 8, as well as for the features that they add.

6. Claim 14

In the rejection of claim 14, the Office Action said to see the preceding argument with respect to claim 1. Applicants respectfully assert that claim 14 is patentable over the cited reference, alone or in combination, for similar reasons to those discussed above with regards to claim 1. Accordingly, Applicants respectfully request that the rejection of claim 14 be reconsidered and withdrawn.

7. Claims 15-16

Claims 15-16 depend from claim 14. Applicants assert that these claims are patentable for at least the reason that they depend from claim 14, as well as for the features that they add.

8. Claims 17-19

Allowable claim 17 has been redrafted in independent form, such that it includes the features of claims 15 and 16. Claims 18 and 19 depend from claim 17. Applicants respectfully request that these claims be allowed.

VI. Conclusion

In light of the above, it is respectfully requested that all outstanding rejections be reconsidered and withdrawn. The Examiner is respectfully requested to telephone the undersigned if he can assist in any way in expediting issuance of a patent.

The Commissioner is authorized to charge the required fees and any underpayment of fees or credit any overpayment to Deposit Account No. 06-1325 for any matter in connection with this reply, including any fee for extension of time, which may be required.

Respectfully submitted,

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